UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,926	09/13/2000	Nobuaki Tokushige	900-348	7467

7590 02/12/2003

Nixon & Vanderhye PC
8th Flooor
1100 North Glebe Rd
Arlington, VA 22201-4714

EXAMINER
HU, SHOUXIANG

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/660,926	TOKUSHIGE, NOBUAKI	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-11 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,4-11 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *28 May 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 5/28/02 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Objections

2. Claims 1, 4-11 and 24, insofar as being supported by elected Species I along with Species II, are objected to because of numerous informalities and/or defects, including but not limited to:

Claims 1 and/or 7 fail to clearly define and/or clarify the following subject matters: (1) the recited source and drain regions and the channel region are formed in the recited semiconductor layer; (2) where the bias voltage is applied to for the second MOS transistor (the gate or the back gate); (3) what it the relationship between the term of "bias voltages" (lines 5-6 in claim 1; or the term of "a bias voltage" in line 7 of claim 7) and the term of "bias voltage" (the third line from the bottom of claim 1 or claim 7); (4) each transistor has its own back gate bias voltage, instead of the "bias voltage for both of the transistors" as recited in claims 1 and 7 (the third line from the bottom); (5) the term of "the transistors" should read as –the first and second transistors--, as the claim is open-ended, and it may further comprise other transistors.

In claims 5 and 9, the term of "the transistors" should read as –the first and second transistors--, as the claim is open-ended, and it may further comprise other transistors. In addition, both claims 5 and 9 fail to clearly define in which layer the well for the second MOS transistor is formed.

Furthermore, in claim 7, the term of "as is the other region" should read as –same as that of the other region–.

In claim 11, it is not clear whether the term of " the MOS transistor" refers to the first transistor or the second transistor.

In claim 8, the term of "the bias voltages" lacks sufficient antecedent basis in the claim.

Claim 24 recites the subject matter that the P-type well and the N-type well are isolated from each other. However, according to Fig. 4(d), these wells are only substantially electrically isolated from each other under certain bias polarities with respect to these wells.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 4-11 and 24 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as

to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Each of claims 1, 7 and 24 recites the subject matter that "the active regions of the transistors are fully depleted simultaneously in the standby state". But, applicant failed to point out where the full support for it could be found in the original disclosure. If the active regions are really **fully depleted**, there should have no leakage current therethrough. However, the original disclosure does not fully support such a subject matter, as it does not disclose that the off-current in the standby mode can be fully eliminated, rather than that the can be "set low" (see page 28, lines 5-8, and page 30, lines 19-24.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-5, 7-9 and 11, insofar as being in compliance with 35 U.S.C. 112, and being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitani et al. ("Mitani"; WO99/27585; also see US 6,392,277 for its English version) in view of 96-12470 (" '470 "; Korean Patent Publication, of record).

Mitani discloses a semiconductor device (see Figs. 8, 16 and 17 in its English version—US 6,392,277), comprising: a first MOS transistor (Qn, n-type) with source and

drain regions (28) in a semiconductor layer formed on a semiconductor substrate (20A; p-type); buried insulating film (20B); and a first contact portion (a left portion of 33D) for applying a first bias voltage to a P-type well (24A), and a second contact portion for applying a second bias voltage to an N-type well (24B) in the substrate underlying a second MOS transistor (Qp, p-type). It is noted that the active regions of the first and second transistors in Mitani can be inherently substantially fully depleted simultaneously in the standby state, as both of them are a complete depletion type (see col. 9, lines 31-34) and the leak currents in them are further reduced in the standby state (see col. 15, lines 41-52).

Although Mitani does not expressly disclose that the contact portion can be formed in a device isolation region, one of ordinary skill in the art would readily recognize that a contact portion can be readily formed in a device isolation region for forming the contact with improved device isolation without wasting additional spaces, as evidenced in '470 (see the contact portion 31 formed in the device isolation region 16 in Fig. (D)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the device isolation region of '470 into the semiconductor device of Mitani, so that a semiconductor device with improved device isolation without wasting additional spaces would be obtained.

Regarding claim 11, the bias voltages in Mitani inherently change the threshold voltages of the first and second transistors (see col. 14, lines 62-66).

6. Claims 6, 10 and 24, insofar as being in compliance with 35 U.S.C. 112, and being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitani et al. ("Mitani"; WO99/27585; also see US 6,392,277 for its English version) in view of 96-12470 (" '470 "; Korean Patent Publication, of record) and/or Burr (US 6,072,217)

The disclosures of Mitani and/or '470 are discussed as applied to claims 1, 4-5, 7-9 and 11 above.

Mitani further discloses that the P-type well and the N-type well are held in a reverse-bias relationship, which inherently implies that the two wells are substantially electrically isolated from each other because of the inherent electrical isolation associated with the p-n junction inherently formed therebetween.

Although Mitani (or, Mitani and '470) does not expressly disclose that the two well can be further isolated, one of ordinary skill in the art would readily recognize that two neighboring wells can be physically spaced apart for better isolation between them, as evidenced in the Burr (see the back gate wells 544 and 546 in Fig. 5).

It would therefore have been obvious to one of ordinary skill in the art at the time the invention was made to make the semiconductor device taught by Mitani (as regarding to claim 24; or, collectively taught by Mitani and '740, as regarding to claims 6 and 10) with the two wells being further isolated, as taught in Burr, so that a semiconductor device with better inter-well isolation would be obtained.

R sponse to Arguments

7. Applicant's arguments with respect to claims 1, 4-11 and 24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703) 306-5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SH
February 6, 2003

Shouxiang Hu
Patent Examiner
TC2800